LISTING OF CLAIMS

This listing of claims replaces all prior versions and listings of claims in the application:

1. (Currently amended): A particularly configurable processor for processing error induced computer programs which are selectively operable on said particularly configurable processor, comprising:

a central processing unit chip;

processor circuitry on said chip;

~~an~~ a programmable error correcting circuit ~~being programmable~~ on said chip;

~~an instruction buffer~~ RAM on said chip ~~for receiving instructions for microprocessor execution memory location for storing an error correction key~~ storing error correcting information, said RAM being in communication with said programmable error correcting circuit; and wherein:

the programmable error correcting circuit ~~controlled at least in part by~~ receives said error ~~correction key~~ correcting information and processor instructions containing errors that are not capable of being executed by said processing circuitry, and

said programmable error correcting circuit generates corrected processor instructions in response to said processor instructions containing errors and said error correcting information, the corrected processor instructions being capable of being executed by said processing circuitry ~~, wherein the control of the error correction circuit permits correction in a predictable manner of intentionally inserted errors in a compiled program provided for execution in accordance with a programmed error correction scheme~~.

2. (Previously canceled).

3. (Original): The processor of claim 1, wherein said error correcting information includes a key that enables selection of error correction specific to ~~the induced error~~ an error scheme used to generate said errors.

4. (Original): The processor of claim 1, wherein information provided in compiled computer program data in part controls said error correction, thereby providing complementary error correction with a combination of the error correction key and the information provided in the compiled computer program data.

5-12. (Canceled)

13. (Currently amended): The processor of claim ~~1~~ 3, wherein ~~data and~~ instructions provided to ~~a computer~~ said processor ~~via program information~~ include an intentional introduction of errors which are correctable with error correction algorithms, said correction algorithms pre-selected according to the key.

14-16. (Canceled)

17. (Currently amended): A microprocessor for processing computer programs which are selectively operable on selected ones of individual microprocessors, comprising:

an integrated circuit chip;

instruction processing circuits on said chip;

~~an~~ a programmable error correcting circuit on said chip~~; a programmable feature on the error correcting circuit, providing a selectability in an error correction scheme to be performed by the error correcting circuit~~; and

a memory location on said chip for storing error correction information, ~~whereby the stored error correction information controls the~~ said programmable error correction circuit ~~feature,~~ selecting an error correction scheme based on said error correction information ~~thereby permitting correction in a predictable manner of intentionally inserted errors in a compiled program provided for execution in accordance with an error correction scheme selected~~; and

wherein said programmable error correcting circuit receives instructions having errors and said error correction information, and said instruction processing circuits process corrected instructions generated by said programmable error correcting circuit.

18. (Currently amended): ~~Method~~ A method for processing a computer program~~s selectively operable~~ on ~~one or more selected individual~~ a microprocessors, the method comprising:

intentionally placing errors in the computer program;

loading instructions of said computer program onto instruction registers on a microprocessor chip;

~~providing an error correcting circuit;~~

storing error correction control information ~~in the form of an error correction key, thereby selecting an error correction scheme for execution in accordance with the key~~ on said chip;

~~compiling program instructions in accordance with the selected error correction scheme, thereby permitting correction in a predictable manner of intentionally inserted errors in a program provided for execution in accordance with the error correction scheme selected; and~~

~~controlling said error correction controlled in part by information provided in compiled computer program data, thereby providing predictable error correction with a combination of the error correction key and the information provided in the compiled computer program data~~

on said chip, correcting said instructions using said error correction control information; and

executing said instructions on said chip.

19-26. (Canceled)